REMARKS

Claims 1-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 5,691,912 (DUNCAN) in view of U.S. Patent 6,516,456 (GARNETT) and U.S. Patent 6,145,117 (ENG). The Examiner is respectfully requested to withdraw the rejection of claims 1-21 in view of the following comments distinguishing each claim over the combination of DUNCAN, GARNETT and ENG.

Claim 1

Relative to claim 1, the Examiner cites DUNCAN as teaching providing a normal display mode displaying a schematic diagram showing components and connection lines interconnecting them. The Examiner also cites DUNCAN as also teaching a topology editing function allowing a user to edit the normal mode display of the schematic diagram and to generate a netlist based on the edited schematic diagram. However the following distinguish claim 1 over the combination of DUNCAN , GARNETT and ENG..

1. DUNCAN fails to teach processing a netlist to generate the normal mode schematic display. The schematic diagram display is generated by a schematic editor 50 (See FIG. 5) based on user input and on data it obtains from a state flow component library 45 and a schematic component library 40, neither of which is a netlist. See FIG. 5 and col. 8, line 30 through col. 9, line 9.

2. As the Examiner correctly points out, DUNCAN fails to teach providing a topology display mode showing components of the schematic diagram without also showing the corresponding connection lines. The Examiner cites GARNETT as teaching a topology display mode wherein a schematic diagram is displayed that includes components but not connection lines. The Examiner points to GARNETT's FIGs. 18-20 as examples of displays of schematic diagrams using the recited topology display mode. However, while FIGs. 18-20 may slightly

resemble schematic diagrams, they are not schematic diagrams but rather depictions of a placement plan for a portion of an IC, showing relative positions of cells within the IC layout. Note also that every one of the placement diagrams of FIGs. 18-20 also includes representations of interconnections to at least one of the cells. Thus GARNETT does not teach the recited topology display mode because FIGs. 18-20 are not schematic diagrams, and because each of GARNETT's FIGs. 18-20 does show representations of at least some connection lines. Also, it would not be obvious to combine DUNCAN with GARNETT's teachings relative to the display of GARNETT's FIGS. 18-20. While claim 1 and DUNCAN are concerned with the display and editing of a representation of a schematic diagram, GARNETT's teachings with respect to FIGs. 18-20 relate to the display of a representation of an IC placement plan.

3. DUNCAN and GARNETT also fail to teach providing the recited editing function "combinable with the topology display mode" enabling a user to modify the relative position or sizing of a selected component" without viewing the connection lines". The applicant's topology mode display is advantageous because by eliminating the connection lines, which clutter a circuit diagram, a user can more easily focus on and adjust the size and position of each component of the schematic. DUNCAN's editing function works only in connection with a display mode in which connection lines are shown. GARNETT does not disclose a topology editing function for editing sizes or positions of components of a schematic diagram displayed in any mode. The Examiner cites GARNETT (col. 8, lines 54-67) as teaching EDA software for editing "component placement and interconnect routing" (i.e., with editing an IC layout) , but this has nothing to do with editing a schematic diagram, as recited in claim 1.

4, Nether DUNCAN nor GARNETT teach allowing a user to switch between normal and topology display modes as recited in claim 1. The Examiner cites GARNETT (col. 19, lines 15-58 and

FIGs. 8A-D) as teaching switching between schematics showing all connections and only some of the connection lines. However, the applicant's claim 1 recites switching between schematic showing all connections and no connections. Moreover the cited sections of GARNETT have nothing to do with displays of schematic diagrams; they relate to displays of placement diagrams.

5. The Examiner incorrectly cites ENG (col. 17, lines 36-45) as teaching automatic pin assignment and routing of connection lines within the displayed schematic diagrams. ENG teaches automatic pin assignments and routing of connections lines, but only within the context of an IC floor plan and layout. It would not be obvious to combine ENG and DUNCAN because their teachings are concerned with very different stages of the IC design process. Whereas DUNCAN is concerned with generating a schematic diagram and a netlist, ENG is concerned with generating an IC layout.

Claim 2

Claim 2 depends on claim 1 and is patentable over the combination of DUNCAN, GARNETT and ENG for similar reasons. Also it should be noted that DUNCAN's netlist is a different kind of netlist. It is netlist used as input to a placement and routing tool generating an IC layout and only indicates the nature of each component along with component interconnectivity. It does not indicate the shape or position of component representations within a schematic diagram.

Claim 3

Claim 3 depends on claim 1 and is patentable over the combination of DUNCAN, GARNETT and ENG for similar reasons. Claim 3 further recites "performing the automatic pin assignment and routing at a time that is after a change is made to the netlist and before entering the normal display mode". DUNCAN teaches producing a netlist after entering a normal display mode. GARNETT and ENG do not teach automatic

pin assignment and routing of connections within schematic diagrams. ENG teaches pin assignment and routing only in connection with IC layouts.

Claim 4

Claim 4 depends on claim 1 and is patentable over the combination of DUNCAN, GARNETT and ENG for similar reasons. Claim 4 further recites "grouping connection lines into classes according to a driver/load characteristic of each connection line". Neither DUNCAN, GARNETT nor ENG describe grouping connection lines into classes. The Examiner correctly points out that all connections lines described by DUNCAN inherently have driver/load characteristics, but nothing in DUNCAN suggests anything about grouping connection lines into classes according to such characteristics. The Examiner cites GARNETT as teaching sorting, filtering and storing nets according to whether they are vectors or scalars, however GARNETT does not teach grouping connection lines into classes according to the recited driver/load characteristics.

Claim 5

Claim 5 depends on claim 4 and is patentable over the combination of DUNCAN, GARNETT and ENG for similar reasons. Claim 5 also recites "providing an abstract display mode that presents on the display representations of ones of said components and a plurality of abstract lines between component representations, each abstract line respectively indicating connectivity of a corresponding one of said classes of connection lines between a first component and another of said components". In other words, the abstract display mode shows a third kind of schematic in which a group of similar connection lines connected between the same pair of components are represented by a single abstract line between component representations. This is helpful because it reduces the clutter of connection lines in a schematic while still allowing it to indicate which components are interconnected. Although two components may in fact be interconnected by a

group of 32 connection lines, only one abstract line is displayed to represent the entire group. The Examiner cites GARNETT (FIG. 4, 138, 140, 144) as teaching selecting cells to be displayed, and selecting the type of net to be displayed, (col. 17, line 42 - col. 18, line 10). But nothing in GARNETT teaches anything about generating the recited abstract display in which a single abstract line represents a group of connection lines having similar driver/load characteristics. Every line in GARNETT's placement display represents one and only one connection line (or net).

Claim 6

Claim 6 depends on claim 5 and is patentable over the combination of DUNCAN, GARNETT and ENG for similar reasons.

Claim 7

Claim 7 depends on claim 6 and is patentable over the combination of DUNCAN, GARNETT and ENG for similar reasons. Claim 7 further recites "providing abstract information on the display for an abstract line, the abstract information indicating the number of driver connection lines and load connection lines in the group of connection lines associated with the abstract line". The Examiner cites GARNETT as teaching generating lists of nets. But generating lists of nets has nothing to do with showing information on a display of an abstract line indicating a number of associated connection lines the abstract line represents.

Claim 8

Claim 8 depends on claim 5 and is patentable over the combination of DUNCAN, GARNETT and ENG for similar reasons.

Claim 9

Claim 9 depends on claim 5 and is patentable over the combination of DUNCAN, GARNETT and ENG for similar reasons. The Examiner cites GARNETT as teaching a combination of abstract mode and topology display mode. However, as discussed

above, GARNETT's displays depict IC placement plans and do not depict circuit schematics. Also GARNETT does not teach a display in which one abstract line represents a group of connection lines.

Claim 10

Claim 10 depends on claim 4 and is patentable over the combination of DUNCAN, GARNETT and ENG for similar reasons. Claim 10 further recites "together connection lines having common driver/load characteristics to form one or more routing groups; for each routing group, utilizing a router to generate a routing line that routes between two components; and splitting the routing line to provide a respective route and pin assignment for each connection line in the routing group." Neither DUNCAN, GARNETT nor ENG disclose such a method of routing connection lines in a schematic, and the Examiner makes no assertion that they do.

Claim 11

Claim 11 depends on claim 10 and is patentable over the combination of DUNCAN, GARNETT and ENG for similar reasons and for reasons set forth above in connection with claim 5.

Claim 12

Claim 12 depends on claim 10 and is patentable over the combination of DUNCAN, GARNETT and ENG for similar reasons and for reasons set forth above in connection with claims 2 and 3.

Claim 13

Claim 13 depends on claim 1 and is patentable over the combination of DUNCAN, GARNETT and ENG for similar reasons. Claim 13 further recites, "the topology editing function comprises a central template auto-arrange function that automatically arranges other components around a user-selected component according to the relative connectivity of the other components with the user-selected component." The Examiner cites GARNETT (col. 4, lines 25-26 and col. 17, lines 26-49)

as teaching such an auto-arrange function, however these lines of GARNETT relate to generating an arrangement of cells in an IC layout and have nothing to do with arranging components in a schematic diagram.

Claim 14

Claim 14 depends on claim 1 and is patentable over the combination of DUNCAN, GARNETT and ENG for similar reasons. Claim 14 further recites, "the topology editing function comprises a fan-in auto-arrange function that automatically arranges other components with respect to a user-selected component according to fan-in connectivity of the other components with the user-selected component." The Examiner cites GARNETT (col. 17, lines 26-41, col. 18, lines 43-72) as teaching such a fan-in, auto-arrange function, however these lines of GARNETT relate to generating an arrangement of cells in an IC layout and have nothing to do with arranging components in a schematic diagram.

Claim 15

Claim 15 depends on claim 14 and is patentable over the combination of DUNCAN, GARNETT and ENG for similar reasons

Claim 16

Claim 16 depends on claim 1 and is patentable over the combination of DUNCAN, GARNETT and ENG for similar reasons. Claim 16 further recites, "the topology editing function comprises a fan-out auto-arrange function that automatically arranges other components with respect to a user-selected component according to fan-in connectivity of the other components with the user-selected component." The Examiner cites GARNETT (col. 21, lines 1-65) as teaching such a fan-in, auto-arrange function, however these lines of GARNETT relate to generating an arrangement of cells in an IC layout and have nothing to do with arranging components in a schematic diagram.

Claim 17

Claim 17 depends on claim 16 and is patentable over the combination of DUNCAN, GARNETT and ENG for similar reasons

Claim 18

Claim 18 depends on claim 1 and is patentable over the combination of DUNCAN, GARNETT and ENG for similar reasons. Claim 16 further recites, "the topology editing function comprises a path auto-arrange function that automatically arranges user-selected components into a path structure, and arranges other components around the user-selected components according to the relative connectivity of the other components with the user-selected components." The Examiner cites GARNETT (col. 19, lines 26-38) as teaching such a path auto-arrange function, however these lines of GARNETT relate to generating an arrangement of cells in an IC layout and have nothing to do with arranging components in a schematic diagram. Also the cited lines of GARNETT discuss only displaying a particular path of nets and has nothing to do with arranging components in an order in which they appear in a path.

Claim 19

Claim 19 depends on claim 1 and is patentable over the combination of DUNCAN, GARNETT and ENG for similar reasons. Claim 19 further recites "providing a line selection function that enables the user to utilize the input device to select a particular connection line; and providing a bus auto-arrange function that automatically arranges the components around a user-selected connection line according to the relative connectivity of the components with the user-selected connection line. Nothing in DUNCAN, GARNETT and ENG discloses the recited bus auto arrange function and the Examiner makes no reference to any section of these references that does. The Examiner cites GARNETT as teaching sorting nets, and

generating lists of nets but these functions have nothing to do with the recited bus auto-arrange function.

Claims 20 and 21

Claims 20 and 21 depend on claim 1 and are patentable over the patentable over the combination of DUNCAN, GARNETT and ENG for similar reasons.

In view of the foregoing amendments and remarks it is believed the application is in condition for allowance. Notice of Allowance is therefore respectfully requested.

Respectfully submitted,

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